Synthesis and Implementation of UART using VHDL Codes

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Abstract— **The proposed paper describes the universal asynchronous receiver/transmitter i.e. UART which is the kind of serial communication protocol which allows the full duplex communication in serial link. This paper presents the hardware implementation of a high speed and efficient UART using FPGA. The UART consists of three main components namely transmitter, receiver and baud rate generator which is nothing but the frequency divider. This has been simulated on ModelSim SE 10.0a and has been implemented by using Verilog description language which has been synthesized on FPGA kits such as Virtex4 and Spartan3.**

Keywords- UART, maximum frequency, number of slices.

I. INTRODUCTION

The universal asynchronous receiver/transmitter is abbreviated as UART. The UART is basically used in between the slow and the fast peripheral devices for example: computer and printer or in between the controller and LCD. Due to this reason, UART is used mostly for the short distance, low speed and is of low cost.

This paper uses the Verilog description language to implement the core functions of UART and integrate them into a FPGA chip. It has three main components i.e. transmitter, receiver and the baud rate generator. As we are using the state machines for transmitter and receiver due to which our design become less complex and the proposed UART becomes more stable, reliable and compact for serial data communication. Due to which, the consumption of LUTs, flip flops or in short the area consumption of the chip becomes less. We have also tested our design for the errors which arises during transmission of data to analyze that our output of the receiver is free from the errors or not. Thus we are tested it for parity and CRC errors.

II. EXPERIMENTAL DETAILS

The three main components of the UART such as transmitter, receiver and the baud rate generator are described below:

A. Transmitter Module:

The function of the transmitter module is to convert the 8 bit serial data into the single bit data. In this module, when our load signal is high the data_in is stored into the holding register. The data in the holding register is shifted to the intermediate register with the start bit of zero and this intermediate register is of 9 bits. Once the shift signal is high the least significant bit of the intermediate register i.e. the start bit comes at the output of the transmitter and served as the input to the receiver. When the entire data has been sent, the transmitter provides a parity bit which is served as the input to the receiver. To check the CRC error, we have to provide the divisor as the user input and once the entire data has been sent, the transmitter generates the remainder which is given as the input to the receiver and receiver provides us the crc_out.

B. Baud Rate Generator

The Baud rate generator is nothing but the frequency divider. In this UART we will apply the synchronized clock signal to both transmitter and the receiver. The clock signal applied to the receiver is 16 times to that of the transmitter.

C. Receiver Module

The function of the receiver module is that it will store the tx_out i.e. the output of the transmitter which is of single bit into the intermediate register with the start bit as the least significant bit and collectively provides the serial data of 8 bit. When the load signal is high it will get the start bit from the transmitter which assures that the original data is now being send by the transmitter. Once the shift signal is becomes high with no load signal, the data coming from the transmitter gets shifted into the intermediate register of the receiver and provides the 8 bit serial data which we have given as an input to the transmitter. Once the entire data has been sent the parity error and the CRC errors has been checked out and are served as the input to the transmitter. If parity error and CRC errors occur or are at logic 1, it means that our transmission is having some errors.

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III. RESULTS AND DISCUSSIONS

The proposed UART has been simulated on the ModelSim SE 10.0a and has been synthesized on the Xilinx ISE 10.1.

A. State Diagrams:

Fig.1 shows the state diagram of transmitter module. The state diagram explains the functionality of the transmitter that how the data has been transmitted. Fig.2 shows the state diagram of receiver module. The state diagram explains the functionality of the receiver that how the data has been received through transmitter

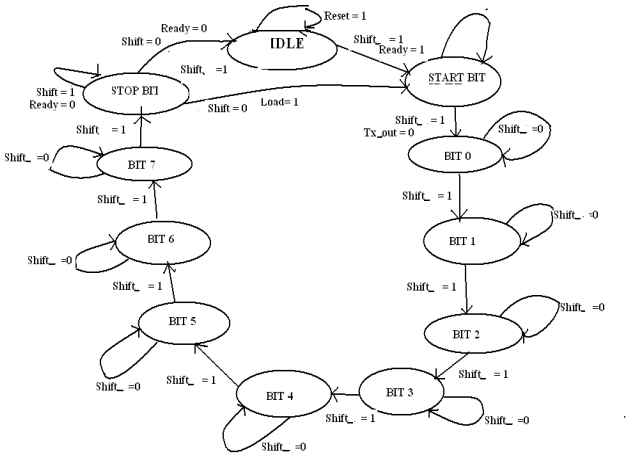

Fig.1 State diagram of transmitter

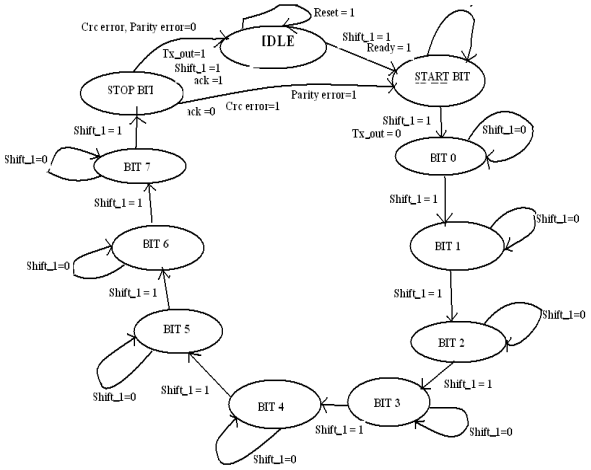

Fig.2 State diagram of receiver

B. Simulation Results

Fig.3 shows the serial transmission and reception of 8 bit data with the maximum frequency of 284.075MHz in case of Virtex4 and 147.710 MHz in case of Spartan3.

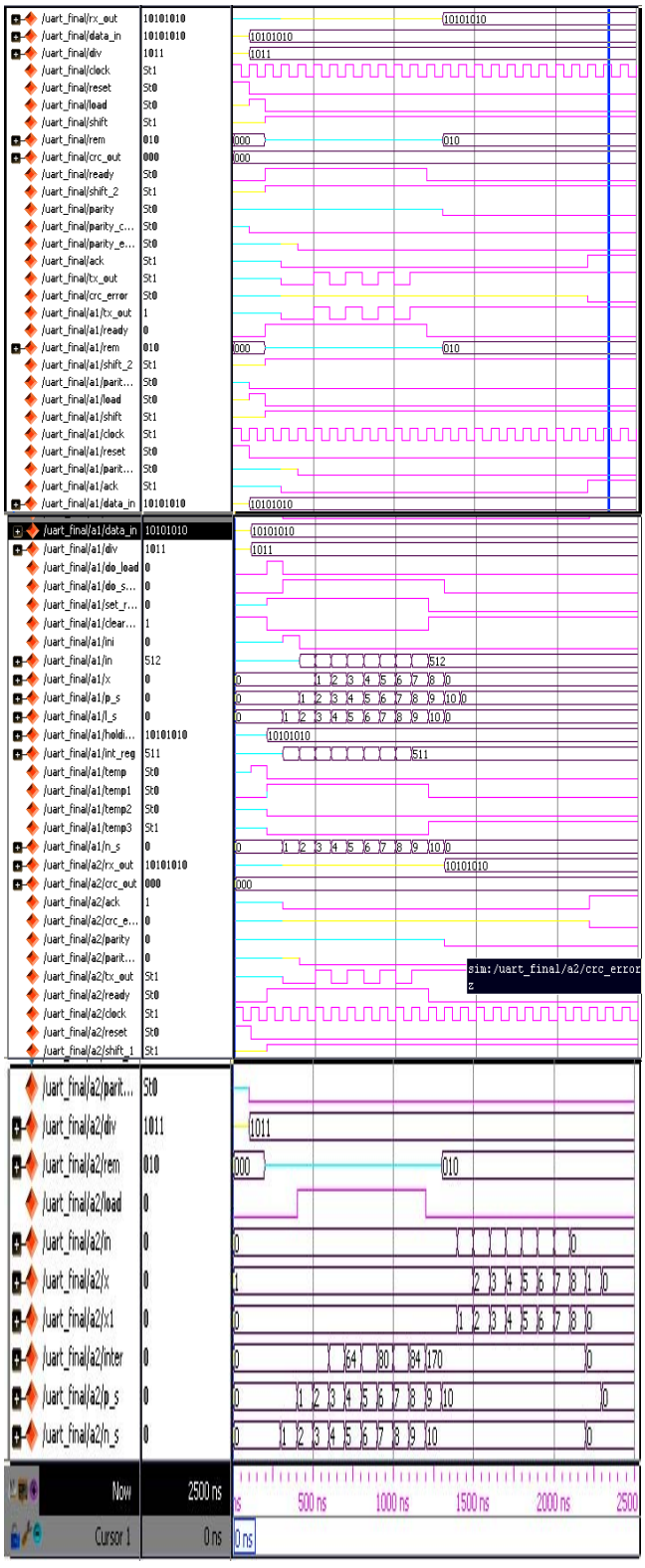

Fig.3 Simulation results of UART

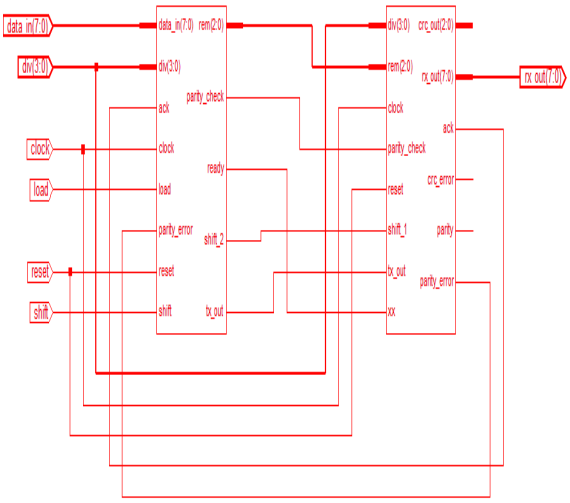

Fig.4 RTL Schematic of UART

C. *Synthesis Result*

The synthesis result contains a table which shows the comparison between the old research and the proposed UART. While doing comparison we will find that our research shows great significance as our all the parameters are consuming less area and consumes less power to operate.

TABLE I.

Serial No.	**Comparison between old research and proposed UART**		
	Parameters	***Virtex4vfx 12sf363-10[4]***	***Virtex4vfx 12sf363-10***
1	Number of slices	63	36
2	LUTs	109	60
3	GCLKs	2	1
4	Slice flip flop	67	46
5	Maximum frequency	289.151 MHz	284.075 MHz

IV. CONCLUSIONS

This uses Verilog description language to get the modules of UART. After studying the comparative analysis we conclude that there is a difference in between the number of slices, LUTs, GCLKs and the maximum frequency. The results are quiet stable and reliable and has great flexibility with high integration. If we use FIFO in making the UART our design becomes more flexible, stable and reliable which provides the high bps rate.

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